A Review on High Performance Asynchronous Delta Sigma Modulator

Mr. Pavan Bhagat
M.E. Student Embedded System and Computing
GHRCE
Nagpur, India
Pavanbhagat158@gmail.com

Prof. Swapnili Karmore
Assistant
Professor
Department of Computer Science and Engineering
GHRCE Nagpur, India
swapnili.karmore@raisoni
.net

***Abstract*— This paper presents the review of work performed in designing of Asynchronous Delta Sigma Modulator. Review considers the use of ADSM for different application. Comparing the performance of different ADSM circuits, a performance criterion is fixed for ADSM design. The performance criteria mainly consider the Low operating voltages, low power consumption, high SNDR and better centre frequency. Then a method is proposed that defines the High performance ADSM that make combined use of different techniques like weak inversion operation and bulk driven MOS for ultra low power design and improving the performance of an Asynchronous Delta Sigma Modulator.**

***Index Terms*— Asynchronous Delta Sigma Modulator(ADSM), Low Power Design, Centre Frequency, Bulk Driven MOSFET.**

I. INTRODUCTION

The advance technology in digital CMOS processes result the increase of the performance in the intrinsic speed of the transistors, give benefits for analog CMOS implementation to obtain high time resolution in the circuit application. Therefore high accuracy CMOS analog circuit can be obtained by using analog signal in time domain circuits instead of the conventional voltage domain [1]. One of the time domain analog circuit implementation is a duty-cycle modulation or asynchronous delta-sigma ($\Delta\sum$) modulator. Synchronous delta sigma modulator uses global clock for synchronization and thus its complexity increases due to synchronization circuitry. Also, it uses a clocked quantizer that introduces an error in output signal. Where as in asynchronous delta sigma modulator, no global synchronous clocked is used thus circuit complexity is reduced. Also lack of clocked quantizer make its output error free[2], but due to presence of hysteresis comparator in a design there is always presence of comparator propagation delay that introduces change in period of output[3] which will be discussed later.

For a long time the term low voltage was significantly used for circuits working under 3V which was significantly low as compared to devices operating at 5v. Later on operating voltages were significantly reduced to 1.8v to 1.2 v with technology scale down process. Scalling down is always not a good choice for lowering operating voltages as it takes a large value to shift
from one process to another[4]. Considering the market trend, a high performance device is typically tested for its operating voltages, frequency responses and power consumption. Speaking fairly, operating voltages and power consumption contribute more for any device. To achieve low operating voltages and low power consumption different techniques like

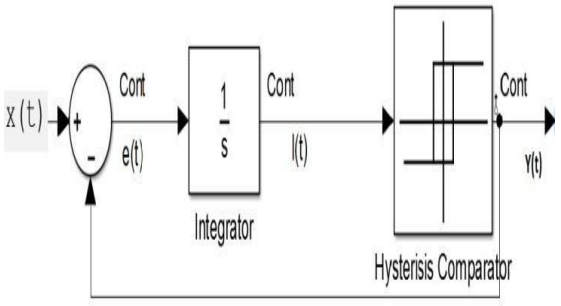

Fig.1: Block Diagram Of Asynchronous Delta Sigma Modulator

subthreshold operation, bulk driven MOS are being used. These techniques allow to operate the devices at comparatively very low voltages with low power consumption.

Use of bulk driven transistor and operating it in weak inversion or subthreshold region is good for low voltage and low power circuits. But there is still problem of reduced *gmb/gm* ratio in Nanometer CMOS technology. This is mainly due to less changed concentration of background doping in different CMOS process [4]. To set the lower threshold voltages , halo implant technique is used. How ever it is reported that use of halo implant to combat short channel effects has anomalously resulted in large drain induced voltage shift and lowering output impedance[8]

The related work about the previous research is explained in section II. Section III & IV describe the research design & proposed architecture of research work. Section V describes a impact of proposed work on existing works undertaken followed by the expected outcome in section VI. Section VII describes the conclusion.

II. RELATED WORK

Fig.1 shows the architecture for ADSM proposed by Roza [1].Lot of work regarding design of asynchronous delta sigma modulator is carried out and little of it focuses on design of very low power and very low operating voltage design. It is found that all the work concerning the low power have implemented bulk driven MOSFET in weak inversion mode. Due to large scaling in CMOS process short channel length effect have been occurred, and different channeling techniques have been reported to mitigate this effect. One of these technique is use of halo implant or pocket implant.

Design of the low power ADSM is based on integrator and hysteresis comparator, where OTA is being a main building block of integrator so many of the researchers give stress on designing the OTA as overall frequency responce of circuit is mainly dependant on frequency responce of OTA. ADSM is widely used in communication system for A/D conversion and requirement of A/D conversion varies from application to application, thus significant changes were noticed in the ADSM circuits.

In[7], an ADSM is designed for biomedical and sensor application operating with energy harvested from environment. For this an ADSM operating at 0.25v at very low power is designed in it. Fig.2 shows architecture for this work. To enable such a low voltage operation it uses approaches that include bulk driven MOSFET operated in weak inversion region. When bulk driven MOSFETs are operated in weak inversion region, transconductance is reduced, thus a technique have been suggested for improving trans conductance in the same. To reduce the operating voltages at present technology, change in dopping concentration is of great importance. Halo implant or pocket implant suggested for this purpose. Use of halo implant have drawback of reduced output resistance.

ADSM designed in this is based on Roza's architecture which forms the close loop system with the integrator and hysteresis comparator. Integrator

implemented is typically a first order integrator that makes use of enhanced Millar OTA. Work done in this gives the operating voltage of 0.25V with modulator centre frequency of 630 Hz. Also, it provides SNR of 62 dB which is quite low and has the scope of improvement. A very interesting and a big achievement made in this is a power consumption. This design typically consumes a very low power of 28 nW which truly a low power design.

In[8], DSM is reported as a duty cycle modulation. For this work DSM is used to perform the Analog to Digital conversion. DSM is widely used for D/A convertors by many researchers as it provides possibility of overcoming resolution problem in low voltage CMOS analog to digital convertors. Work performed here shows the very basic and detailed design for DSM. Still, many factors are remained to be

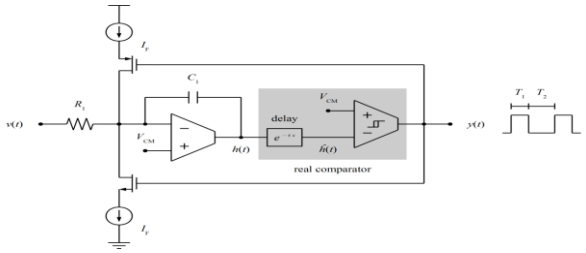

Fig. 2: Circuit Implementation Of ADSM

address which are necessary for circuits in deep submicron region. Design proposed in this scheme is typically a Analog-to-Digital convertor that makes use of Asynchronous Delta Sigma Modulator whose design is appreciable. ADSM given in this literature is designed for a high band width requirement systems typically like a DSL. But due to synchronous operation, circuit complexity of this architecture is high.

This DSM design typically operates at 1.8V and consumes 1.8mW of power. Design is implemented by using the second order integrator that leads it to more power consumption but with the benefit of better SNR of 70 dB and higher centre frequency. This work mainly focuses on Time-to-Digital-Convertor (TDC) and improvement in TDC for lossless reconstruction of information rather than focusing on DSM, but DSM implemented is of better performance and thus we found interest in it.

In[10], compareson of different analog to digital conversion is performed. Detailed comparison of different A/D convertor schemes mainly Nyquist limit based ADC and oversampling based ADC. When Nyquist rate based ADC are considered, they extensively use clocked quantizer thus quantizer noise is always present at the output . When oversampled ADC is considered, instead of using quantizer it uses hysteresis comparator and whatever the noise generated is spread over the wide frequency range in the output and thus oversampled

ADCs are also referred as noise shaping ADCs. Furthermore as operating voltages are reducing, this creates problem in output resolution in time domain.
On the other hand, in oversampled ADC mainly in ADSM based ADC analog input is converted into continuous time but discrete amplitude output signal. That means, amplitude axis is replaced by time axis, and due to availability of very fast CMOS devices we have good resolution over time axis[9].

In ADSM, hysteresis comparator is basic building block and centre frequency of ADSM completely depends on the hysteresis comparator propagation delay. Propagation delay is the time for which integrator integrates input signal and the integrator output overcomes the hysteresis level. If this propagation delay is large then centre frequency is small and ADSM performance degrades. If this overshoot remains in system then it

will spread the period of output [3]. Thus propagation delay must be kept as low as possible for improved centre frequency.

Based on the study of different Asynchronous Delta Sigma Modulator presented in [7][9][10] with different application following comparison is carried out. A suitable design will be develop with the advantageous sets of design of different architectures.

III. PROPOSED SYSTEM

Table 1: Performance comparison between different schemes

	[	[	[
Technolo	130 nm	0.18 um	0.18um
Power Supply	0.25 v	1.8 v	1.8 v
Topolog	ADSM	DSM	ADSM
Order	1st	2nd	1st
Input Type	Single ended	Single ended	Single ended
Modulator	630 Hz	2 GHz	140MHz
	30 Hz	1.23	--
SNR	62 dB	79 dB	70dB
Power Consump	28 mW	1.8 mW	1.5 mW

All the ADSM architectures compared above are based on Roza's architecture[1].So architecture for our work will also be based on Roza's architecture. Proposed system is first order clock less system that's why it is called asynchronous. It is a close loop system consisting of an integrator and a hysteresis comparator. Roza's architecture shows large propagation delay which will be minimized by techniques in [7].As seen from the comparison table all different architecture are proposed for the different application requirement such as [7] is specifically designed for the biomedical application with very low frequency signal eg. Signals for pace maker, but this operates at tremendously low voltage of 0.25V and extremely low power of 28nW. In[8] as depicted from table 1, modulator centre frequency is very high and in [10] it better than [7]. So there is a scope of improvement in centre frequency in [7] where[8],[3] suffers from operating voltages and power consumption that can be optimized with achieving high SNR.

IV. CONCLUSION

Thus, here different ADSM architectures are discussed which are mainly concerned with particular application. Looking at the good sides of different application, a generalized architecture can be developed with combining the good results of all architecture in a suitable way. Based on this, a system will be developed that will operate at 0.25V and with the minimum possible power consumption. A system will also try to minimize the propagation delay of hysteresis comparator so that centre frequency can be suitably kept high that allows the use of architecture for wide range of applications

ACKNOWLEDGEMENT

The research work presented in this paper was done by Pavan Keshao Bhagat student of 3rd Sem in Embedded System & Computing. The proposed research is ongoing under the guidance of Prof. Swapnili karmore.

REFERENCES

[1] E. Roza, -Analog-to-digital conversion via duty-cycle modulation,‖ *IEEETrans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 44, no. 11, pp. 907–914, Nov. 1997.

[2] J. Daniels, W. Dehaene, M. S. J. Steyaert, and A. Wiesbauer, -A/D conversion using asynchronous delta–sigma modulation and time-to-digital conversion,‖ *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2404–2412, Sep. 2010.

[3] Tomislav Mati´c, Tomislav Švedek, *Member, IEEE*, and Marijan Herceg, -A Method for the Schmitt-Trigger Propagation-Delay Compensation in Asynchronous Sigma–Delta Modulator‖, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 59, NO. 7, JULY 2012.

[4] Luís H. C. Ferreira,and Sameer R. Sonkusale,―A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process‖, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 61, NO. 6, JUNE 2014 160.

[5] Shouri Chatterjee, Yannis Tsividis,and Peter Kinget, -0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design‖ IEEE Journal Of Solid-State Circuits, Vol. 40, No.12, December 2005.

[6] Luís H. C. Ferreira,and Sameer R. Sonkusale, -A 0.25-V 28-nW 58-dB Dynamic Range Asynchronous Delta Sigma Modulator in 130-nm Digital CMOS Process‖,

[7] Jorg Daniels, Wim Dehaene, Michiel S. J. Steyaert, and Andreas Wiesbauer. "A/D Conversion Using Asynchronous Delta-Sigma Modulation and Time-to-Digital Conversion‖,IEEE Transactions on Circuits and Systems-I Regular Papers, Vol. 57, No. 9, September 2010.

[8] S. Chakraborty, A. Mallik, C. K. Sarkar, and V. R. Rao, -Impact of halo doping on the subthreshold performance of deep submicrometer CMOS devices and circuits for ultralow power analog/mixed-signal applications,‖ *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 241–248, Feb. 2007.

[9] Pervez M. Aziz, Henrik V. Sorensen, And Jan Van Der Spiegel , -An Overview Of Sigma Delta Convertors‖, IEEE Signal Processing Magazine, January 2010.

[10] S.Ouzounov, E.Roza*, H. Hegt, G.van der Weide* and A. van Roermund, -An 8MHz, 72 dB SFDR Asynchronous Sigma-Delta Modulator with 1.5mW Power Dissipation‖, Symposium On VLSl Circuits Digest of Technical Papers 2004.