A Survey Report for Design of FIR Filter

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ABSTRACT:

A FIR filter is an important element in digital signal processing. This removes noise from the signal and improves efficiency of the signal. There is lots of work done on design techniques of FIR filter. Area and power efficiency are the important design issues. Every technique has its own advantages and disadvantages.This proposed paper gives review of such different techniques proposed earlier in literature.

Keywords: finite impulse response (FIR) filters, Digital signal processing (DSP), area efficiency, power efficiency.

I. INTRODUCTION

Filter is a networkwhich passes signal with certain frequencies and reject the signal with other frequencies thus it does not change the frequency of signal, only change amplitude of frequency component. Finite Impulse Response (FIR) filters are of great importance in Digital Signal Processing (DSP) systems.Finiteimpulse response filter (FIR) is most popular filter because it having linear characteristics and no feedback is required giving most stable operation. Low area and low power are the main issues of the FIR filter design, because of its wide application in signal processing and communication systems.

Multiplier is more area consuming element in FIR filter, due to this most of designs are divided into multiplier less and memory based designs with different approaches. In this paper study of advantages and dis advantages of various approaches is mentioned.

II. LITERATURE SURVEY

In the last two decades, there are many efficient algorithms and architectures have been introduced for the design of low cost FIR filter.

Vaidyanathanworked onarchitectural transformations techniques for low power design. He suggested hybrid encoding which is middle way between minimal inputdependency of binary coding and the low switching characteristic of the gray encoding..This hybrid encoding technique saves power upto 25% and also gives increase in delay about 14%.And area increase of 28%.On comparing binary coding and hybrid coding for pipelined architecture we get results showing higher area for architectures with Hybrid operators, presenting less minimum clock period and energy per sample [1].

Lu implemented digital filter as cascade arrangement of low order sections. In which he design first sectionthrough optimization, and then addedfixed and a second sectionsatisfying required specifications. He was repeated this process still multi section filter is obtained. Filter of this type requires minimum number of sections to process the current input due to use of adaptation mechanism giving low power consumption [2]

Meher et al.presented the design which is memory based. Using look table and distributed arithmetic. Lookup table's offers flexible choice of address length for DA based computation. This offers trade of between area and time.Selection of smaller address length reduces memory requirement.But this cause increase of adder complexity and the latency [3].

Phuong design FIR filter using window method. Specification of FIR are in discrete time domain in which impulse response is design objective or in frequency domain in which design objective is magnitude response or both. In all fixed windows Kesar window was adjustable length (M+1) but it has an additional ripple factor

which causes trade of between transition and ripple [4].

Kamaraj et al.suggested use of HDL language in FIR filter design which improves speed of the system.Also suggested use of the pipelining technique in which multiple instructions executed parallaly.Thus proposed design gives improved speed in lower cost and low hardware also gives high operating frequency without disturbing performance [5].

Jiang et al. design FIR filter using FPGA.In which he used Matlab to find out filter coefficients. In this he uses VHDL to design 16 order constant coefficients FIR filter. Simulation is done on Quartus-2 [6].

Li implemented 60-order FIR filter based on FPGA hardware. They used distributed algorithm and its several structures. Inthis multiplication is converted into look up table structure andimplementmultiplication operation. Platform. This filter gives good performance and the speed is higher and the
Resources required are fewer [7].

Rajput et al.designed a FIR filter using modified booth multiplier and Baugh-Woolley multiplier to perform multiplication operation on signed numbers.The modified BoothEncoder circuit generates half the partial products in parallel.To increase the speed of the multiplier he suggested use of Carry Save Adder (CSA) tree and the final Carry Look Ahead (CLA) adder. This suggested design gives less power consumption and reduced area because same multiplier hardware is used to multiply sign and unsigned numbers [8].

Martinez-Peiro et.al.he suggested high-speed multiplierless filters using a nonrecursive signed common subexpression algorithm" .in this he used nonrecursive signed common subexpression elimination algorithm. This algorithm allows using each sub expression once and helping to overcome the problem of a high logic depth into the digital structure. they also compare this technique with other well-known technique one is the graph synthesis, and the other is classical common subexpression elimination technique and the result shows best relation between occupied area and logic depth respect to the previous values given in the technical literature [9].

Chip-Hong et. al.design a FIR filters using multiroot binary partition graph (MBPG) to reduce complexities of digital filter. In this he partitioned the set of coefficients into symbols. Which make common subexpression identification and elimination harmonious to information parsing for data compression. For coding of coefficient they uses less number of different pairs or groups of symbols and residues based on their probability and conditional probability of occurrence. This promises fine grain optimization such as shift-inclusive computation reordering to minimize the width of every two's complement adder which further reduces implementation cost and critical path delay [10].

H.-J. Ko et. al.designed FIR filter using faithfully rounded truncated multiplier. Which gives area reduction and low cost design by removing unnecessary partial product bitsusing deletion, reduction, and truncated.Error produced is also small [11].

III. CONCLUSION

In this paper, we take review of work done in FIR filter design and their advantages and dis advantages about each method. Asarea, power and delay reduction are the major issues for the FIR filter design, most of the designs are based on reducing these three factors.

As the scale of integration keeps growing it required more and more complicated signal processing systems are being implemented on a VLSI chipwhich requires more area and power efficient FIR filters with less delay and less cost.

The future work is to develop a technique which is area efficient and power efficientsuitable for above requirement.

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