"Design of FPGA's High Speed Configurable Logic Units"

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Abstract:
This paper presents the research and design of FPGA's high speed configurable logic unit under 22nm technology. The keystone is the design of FPGA's two basic elements – look-up table(LUT) and configurable register. Decoding circuit and CMOS transmission gate (TG) is applied to build LUT to solve the problems brought by the VDSM technology, such as the low power supply voltage and comparatively high threshold voltage loss. CMOS TG and designed control circuit is used to implement the complex function of FPGA's configurable register to reduce the critical path's delay. Experimental result shows the achieved speed is comparable and even faster than Xilinx's Virtex4 & 65nm tech while retaining small leakage power and area.

1. Introduction:

FPGAs have recently benefited from process advances to become significant alternatives to ASICs. The most common FPGA architecture consist of an array of configurable logic block, IO pads & routing channel[1-5]. In the interior of the CLB there are number of LUT, configurable resistor, multiplexers. In the interior of a CLB, there are several basic units, such as LUTs, configurable registers, multiplexers and some other logics. FPGA's area, speed and power characteristics are mainly affected by CLB's LUTs and configurable registers. Although FPGA is a kind of mature commercial device with wide application, there aren't many open literatures on the research and design of FPGA's internal logic units. On the other hand, for the last decades, there aren't significant changes in CLB's structure [1-4]. The main development of CLB is the increase of LUTs' and configurable registers' number and LUTs' size with the shrink of technology's feature size. More and larger LUTs and configurable registers can increase the granularity of CLB, thus can decrease the delay of interconnect among CLBs, which occupy a significant percentage of the total delay [4]. In this paper, we'll focus on the design of FPGA's LUT and configurable register under 22nm technology, regarding the speed, area, power leakage and reliability. The goal of this work is to design and evaluate programmable logic using 22nm.

2. Circuit Design:

Fig.1 shows the basic structure of FPGA's CLB [1-4], which is mainly uses a couple of 4 input LUTs, registers and some multiplexers. CLBs perform user specified logic functions and interconnect resource carry signals among the blocks. A look up table is an array that replaces runtime computation with a simple array indexing operation. A register is a group of flip-flops or latches that stores a bit pattern & used for I/O synchronization. There are also some auxiliary multiplexers to expand CLB's function. The main differences between FPGAs of different vendors or different series are the number of LUTs and registers and the size of LUT [1-3].

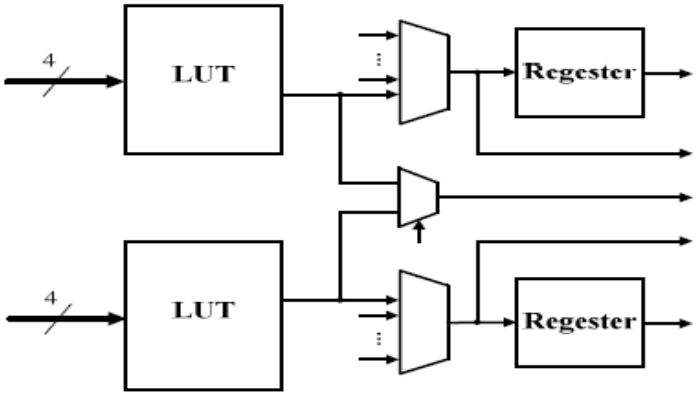

Fig.1 Basic Structure of CLB

2.1 Design of LUT

A simple LUT can be designed using an array of SRAM programmable points and corresponding decoding circuit. A simple 3-input LUT with TG tree is shown in Fig.2, from which it can be seen that every increase of the number of LUT's inputs will double the number of SRAMs. So the commercial FPGAs use 4 to 6 inputs LUT [1-3] to balance the area and speed performance.

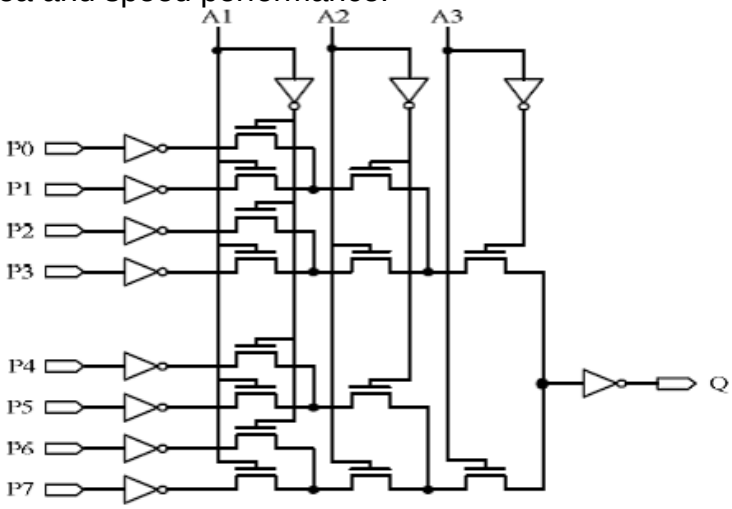

Fig 2. Simple 3 Input LUT Structure

To avoid the problem due to the impact of threshold voltage loss, a possible method is increasing the NMOS TG's gate voltage. However, it will increase the circuit's complexity and decrease the transistors' lifetime. Another feasible solution is using CMOS TG to replace NMOS TG, but it will double the layout area. To solve these problems, a new LUT's structure is proposed and shown in Fig.3

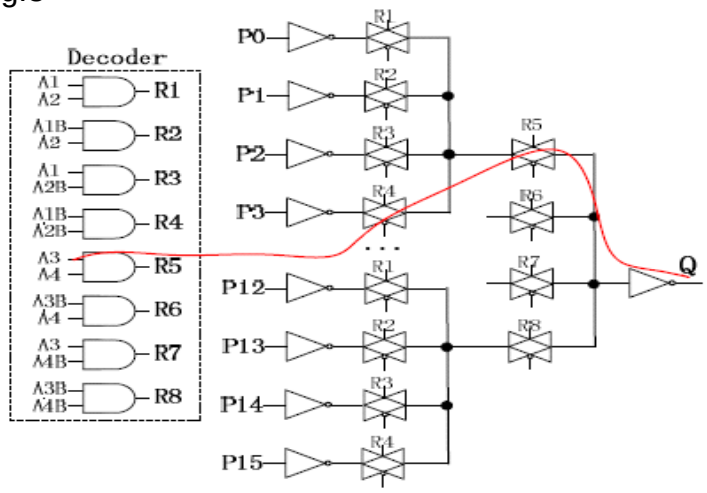

Fig.3 Proposed LUT Structure

In Fig.3, A1, A2, A3, A4 are the four input ports of the 4-input LUT while *A1B, A2B, A3B, A4B* are the inverted signals respectively. P0 to P15 are the 16 outputs of LUT's 16 SRAM programmable points. *A1, A2, A3, A4* select an SRAM's output to Q through the two-level CMOS TGs. Every state of {*A1, A2, A3, A4*} will select one SRAM's output to Q. There are 24 states of {*A1, A2, A3, A4*} in total, perfectly matching the 16 SRAMs of an LUT. In this way, it can act as a 4-input look-up table. In Fig.3, the critical path for any input state is virtually the same. One of the critical path is shown in Fig.3 by the red line, which contains an AND gate, 2 level CMOS TGs and an inverter merely, so the LUT's speed can be very fast. In addition, the use of CMOS TGs to replace NMOS TGs can avoid the problems brought by threshold voltage loss. Decoding circuit is used instead of TG tree to shorten the critical path and lower the required number of transistors, thus smaller layout area can be achieved. As a rule, to get symmetrical rise and fall delay, the size of PMOS transistor is usually double to triple to the NMOS transistor's size. However, too large PMOSs will greatly increase the layout size of LUT. Therefore, the selected PMOS' size in our design is equal to the size of NMOS gate. In the proposed LUT structure, SRAMs P0 to P15 aren't in the critical path, so high threshold voltage transistors are used to decrease the

leakage power while low threshold voltage transistors are used in the critical path to increase the speed.

The circuits' layout is designed using a 22nm, 0.7V low leakage technology and shown in Fig.4 Simulation is done using Microwind 3.5 simulation tool. The Layout area, simulated delay and leakage power under 0.7V, 27°C, are listed in table1 for proposed LUT structure. From this , it can be found that the designed LUT's speed is comparable to Xilinx Virtex7. At the same time, both the area and leakage power are very small.

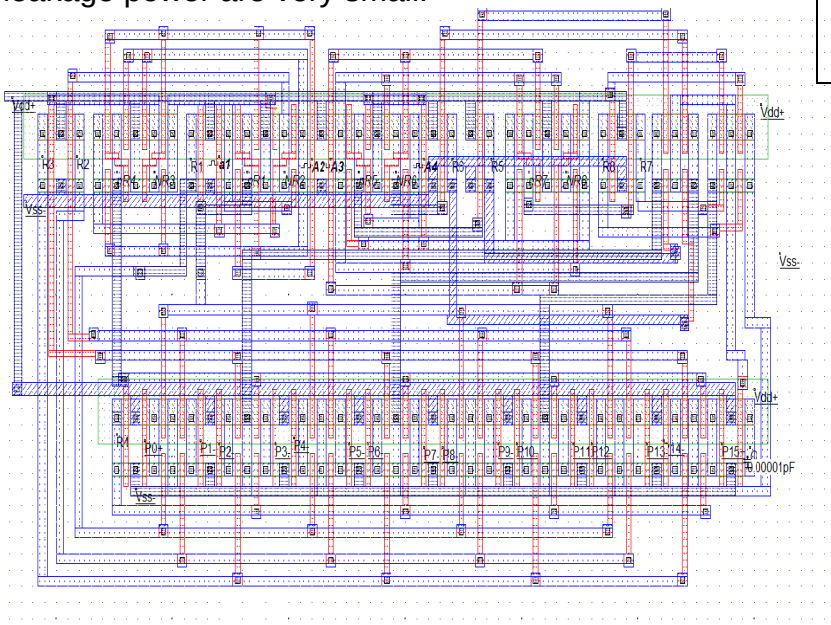

Fig.4 Simulation of LUT

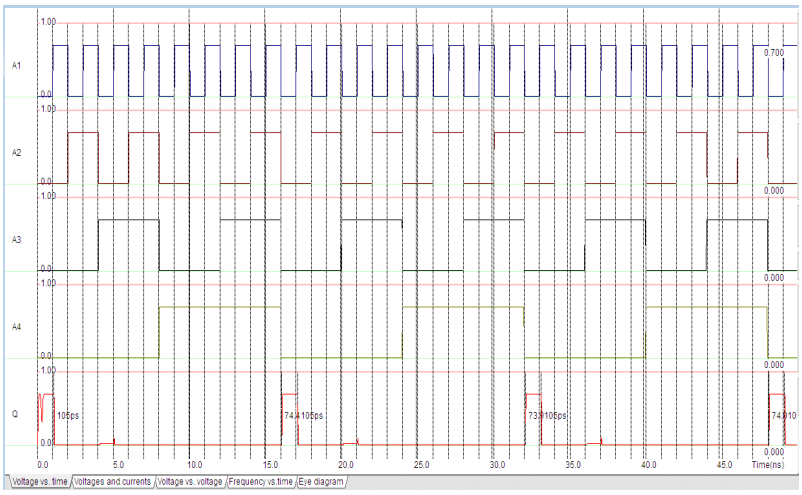

Fig.5 Simulation Results of LUT

Parameters	VDSM (65nm)	VDSM(22nm)
Propagation Delay	LUT–0.17ns Config.Register-0.15ns	0.089ns
Area	14.4*7.2 um2	4.5*2.2 µm2
Leakage Power	LUT – 26 nW Config. Register-11 nW	0.7nW
Technology used	65 nm	22 nm

Table 1. Work Analysis

2.2 Design of Configurable Registers

In FPGA, the main function of a configurable register includes the selection of DFF or latch mode, synchronous or asynchronous set and reset, enabling and so on [1-5]. The function of synchronous set/reset and enabling can be realized by the following expression:

$$PM = R(S + E*Q + E*D) \quad (1)$$

Where *R* and *S* are register's reset and set input port respectively, *E* is the enabling input port, D is the data input port, Q is the register's output port, PM is the signal sent to DFF's main body circuit (shown in Fig.5). The delay of input signal 'D' will affect the register's setup time, so an improved transistor-level circuit of input data control circuit is designed to shorten the input signal's delay, as shown in Fig.4, where the input data control circuit is combined with the first stage of DFF's main body circuit to shorten the critical path delay and decrease the required transistors. Compared to gate level circuit, the critical path of input signal 'D' is decreased from the sum of two AND gates and a NOR gate to a single transistor.

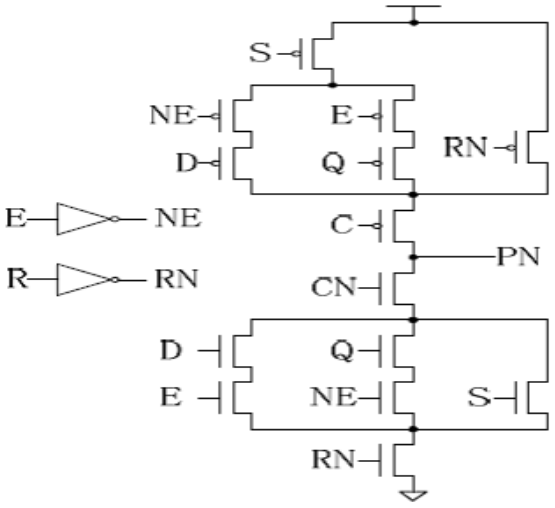

Fig.6 Improved Transistor Level Circuit

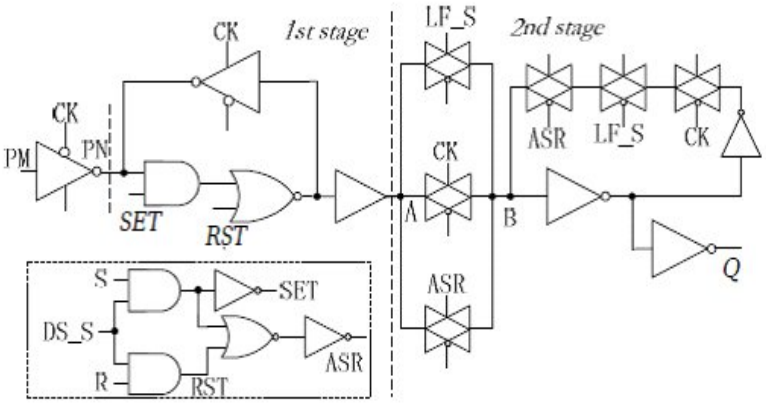

Fig.7 Configurable Register's Main Body Circuit

The main body circuit of the proposed configurable register is shown in Fig.7. It will realize the function of asynchronous set and reset, selection of DFF or latch mode. To get smallest delay from rising *CK* to *Q* (Tck-q), those control logics are moved to non-critical path. In Fig.7, *DS_S* and *LF_S* are the output signals of programmable SRAM points. *DS_S* is used to implement the selection of synchronous or asynchronous mode while LF_S is used to implement the selection of DFF or latch mode. The circuit's work principle is as follows:

when LF_S is '1', point B is equal to point A and the feedback path is cut down, the circuit works as a low voltage transparent latch; when LF_S is '0', the circuit works as a positive edge sampling flip flop. When DS_S is '1', S(R) port sets (resets) both the first stage and the second stage asynchronously; When DS_S is '0', S(R) port is prevented to set (reset) the main body circuit asynchronously, but it can set (reset) the input signal through the input data control circuit synchronously. As the asynchronous set/reset logic and DFF/latch selection circuit are both on the non-critical path, the critical path delay Tck-q can be very small. At the same time, the required transistors are few. Excepting for the output buffer, there is no need for large size transistors, so the layout area can be decreased.

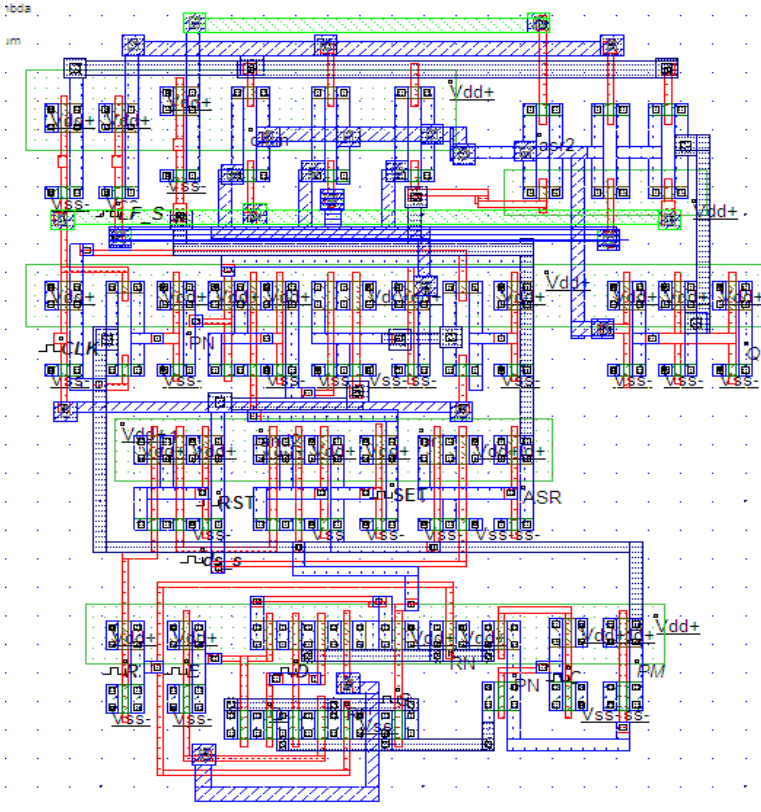

Fig.8 Simulation of Configurable Register

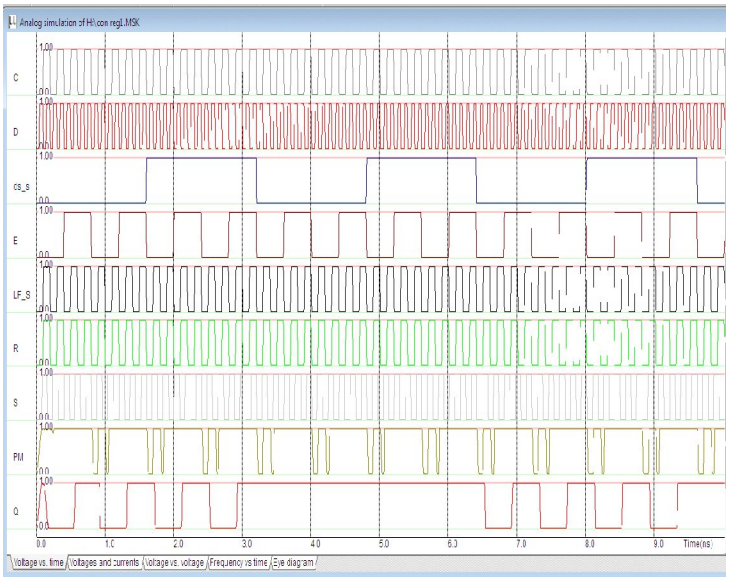

Fig.9 Simulation Results of Configurable Register

3. Experiment Result:

A 4-input configurable LUT is proposed which increases the logic utilization and the flexibility of configuration. The interface of configurable logic block remains the same so the complexity of interconnect structure won't be raised as we used transmission gates. Simulation results show a significant speedup in carry performance over current architecture

Here we have made modifications in LUT of FPGA and implemented same Configurable register design in 22nm technology .This has resulted into improved results as compared to previous work. A high speed LUT for FPGA is designed using 22nm, 0.7V low leakage technology. With reference to the previous ? ???[1], it can be noted that area is reduced by approximately 90%, leakage power by 97% and delay is reduced by 47%. Thus speed of our design is twice higher than previous work.

4. Summary

A novel LUT and configurable register for FPGAs is designed using a 22nm, 0.7V low leakage technology.Great speed performance is achieved while retaining small layout area and leakage power.

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